

Reducing Switching Losses in Cascaded Multilevel Inverters Using Hybrid-Modulation Techniques

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ABSTRACT : *This paper presents four different sequential switching hybrid-modulation strategies. Hybrid-modulation strategies represent combinations of fundamental-frequency modulation and multilevel Sinusoidal-modulation (MSPWM) strategies, and are designed for performance of the well-known alternative phase opposition disposition, phase-shifted carrier, carrier-based space-vector modulation, and single-carrier sinusoidal-modulations. The main characteristic of these modulations are the reduction of switching losses with good harmonic performance, balanced power loss dissipation among the devices with in a cell. MSPWM and its base modulator design are implemented on a TMS320F2407 digital signal processor (DSP). The proposed modulations can be easily extended to three phase, and higher level inverters, operates with same physical structure of the power module. The feasibility of these hybrid modulations are verified through spectral analysis, power loss analysis, simulation, and experimental results.*

Keywords: *Cascaded multilevel inverter (CMLI), digital signal processor (DSP), harmonic analysis, hybrid modulation, power loss analysis.*

I. INTRODUCTION

Multilevel inverters (MLIs) are finding increased attention in industries as a choice of electronic power conversion for medium voltage and high-power applications, because improving the output waveform of the inverter reduces its respective harmonic content and, hence, the size of the filter used and the level of electromagnetic interference (EMI) generated by switching operation [1]. Various multilevel inverter (MLI) structures are reported in the literature, and the cascaded MLI (CMLI) appears to be superior to other inverter topologies in application at high power rating due to its modular nature of modulation, control and protection requirements of each full bridge inverter (FBI) [2]. CMLI synthesizes a medium voltage output based on a series connection of power cells that use standard low-voltage component configurations. This characteristic allows one to achieve high-quality output voltages and input currents and also outstanding availability due to their intrinsic component redundancy [3]. The power circuit for a five-level inverter topology is shown in Fig. 1 used to examine the proposed modulation techniques. Many new modulations have been developed to cater the growing number of MLI topologies. They are aimed at generating a stepped switched waveform that best approximates an arbitrary reference signal with adjustable amplitude, frequency, and phase fundamental component that is usually a sinusoid in steady state. Since the modulation scheme is intended to be used in high-power converters, the main figures of merit pursued are high power quality and minimum switching frequency. These two requirements compete with each other, and therefore, it is considered one of the major challenges in MLI technology [4]. Most of the modulation methods developed for MLI is based on multiple-carrier arrangements with pulsewidth modulation (PWM). The carriers can be arranged with vertical shifts (phase disposition, phase opposition disposition, and alternative phase opposition disposition (APOD) PWM), or with horizontal displacements (phase-shifted carrier (PSC) PWM) [5]. Space-vector modulation (SVM) is also extended for the MLI operation, offers good harmonic performance [6]. These high-frequency methods produce high-frequency stepped voltage waveforms that are easily filtered by the load and, therefore, present very good reference tracking and low current harmonic distortion. However, this is also the reason for high switching losses, which is undesirable in high-power applications. As a result, fundamental-frequency modulation methods have been preferred. Selective harmonic elimination (SHE) has the advantage of having very few commutations per cycle and is, therefore, the one that achieves better efficiency [7]. Nevertheless, offline calculations are

necessary, making dynamic operation and closed-loop implementation not straightforward. In addition, SHE becomes unfeasible with the increase of the number of levels, since it is directly related to the number of angles, hence equations that need to be solved.

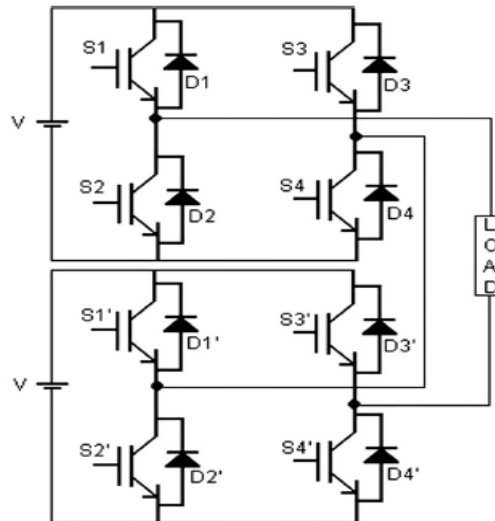


Fig. 1. Schematic diagram of the inverter topology used to verify the proposed hybrid modulations

II. REVIEW OF MSPWM SCHEMES

Unipolar carrier-based N-level PWM operation consists of $(N - 1)/2$ different carriers, same as the number of FBI cells ($K = (N - 1)/2$). The carriers have the same frequency f_c , the same peak-to-peak amplitude A_c , and disposed. The major MSPWM schemes: APOD, PSC, carrier-based SVM (CBSVM), and single-carrier sinusoidal modulation (SCSPWM) are reviewed. Fig. 2 shows the sinusoidal reference and carrier signals for five-level PWM operation. The modulation index for MSPWM is defined as $M = A_m/K A_c$. The modulation frequency ratio is given as $m_f = f_c/f_o$, where f_o is fundamental frequency. For APOD, all carriers are phase opposition by 180° from its adjacent carrier. SCSPWM is a result of multiple sinusoidal-modulating signals with a fundamental frequency f_o and amplitude of A_m and one carrier signal [11]. For N-level SCSPWM, K numbers of modulation signals have the same frequency and amplitude with dc bias of A_c , as a difference between these signals. PSC modulation is to retain sinusoidal reference waveforms for the two phase legs of each FBI that are phase shifted by 180° and to then phase shift the carriers of each bridge to achieve additional harmonic sideband cancellation around the even carrier multiple groups [12]. The carriers for five-level PSC-PWM is defined as

$$C'_1 = A_c y_c(f'_c, 0)$$

and

$$C'_2 = A_c y_c(f'_c, \pi/2) \tag{1}$$

Where $f'_c = f_c/4$. The carriers are shifted by $2\pi/(N - 1)$ incrementally. The normalized Triangular carrier y_c is

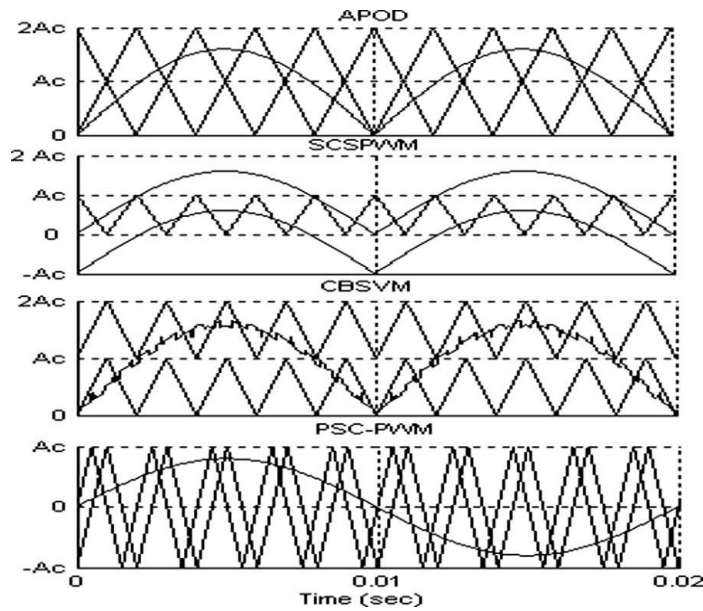


Fig. 2. Sinusoidal reference and carriers of MSPWM operation

Mathematically defined as

$$y_c(f_c, \varphi) = (-1)^{|\theta|}(\theta \bmod 2) - 1 + \frac{1}{2}, \quad \theta = \frac{2\pi f_c t + \varphi}{\pi} \quad (2)$$

Where ϕ represents the phase angle of carrier. SVM is intrinsically a digital technique for generating switching angles, offers relatively good performance at low modulation ratio. But, the SVM becomes very difficult to achieve when the levels increases. To simplify the SVM, several methods have been proposed in recent years: such as decomposing the multilevel SVM to two-level SVMs [13], implementing the SVM in a 60° coordinates [14]. However, it is complex in some steps yet, such as selection of switching-state. Some techniques using common-mode injection in MSPWM are developed to close to SVM [15]. Yao et al. suggested that these techniques are harmonically equivalent, with the best spectral performance being achieved when the nearest three space vector states are selected with the middle two vectors centered in each half carrier switching interval [16]. This strategy is known as CBSVM. It is derived from the addition of a common offset voltage to the three phase references. The offset voltage V_{off} for multilevel operation can be calculated as

$$V_{\text{off}} = -\frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2} \quad (3)$$

$$V'_k = (V_k + V_{\text{off}} + V) \bmod \left(\frac{2V}{N-1} \right), \quad k = a, b, c \quad (4)$$

$$V'_{\text{off}} = \frac{V}{N-1} - \frac{\max(V'_a, V'_b, V'_c) + \min(V'_a, V'_b, V'_c)}{2} \quad (5)$$

The modified phase references are obtained by adding V_{off} and V'_{off} to the reference waveform V_a , V_b , or V_c .

III. PROPOSED SEQUENTIAL SWITCHING HYBRID MODULATION

(A) Basic Principle of This Modulation

Hybrid modulation is the combination of fundamental frequency modulation (FPWM) and MSPWM for each inverter cell operation, so that the output inherits the features of switching-loss reduction from FPWM, and good harmonic performance from MSPWM. In this modulation technique, the four switches of each inverter cell are operated at two different frequencies; two being commutated at FPWM, while the other two switches are modulated at MSPWM, therefore the resultant switching patterns are the same as those obtained with MSPWM. A sequential switching scheme is embedded with this hybrid modulation in order to overcome unequal switching losses, and therefore, differential heating among the power devices. A simple base PWM circulation scheme is also introduced here to get resultant hybrid PWM circulation makes balanced power dissipation among the power modules. Fig. 3 shows the general structure of the proposed SSHM scheme. It consists of modulation base generator, base PWM circulation module, and hybrid-modulation controller (HMC) to generate new modulation pulses Switching hybrid modulation.

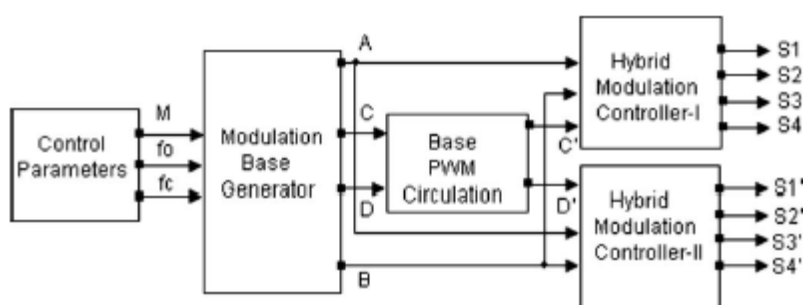


Fig 3: Scheme of proposed sequential

(B) Base-Modulation Design

In this modulation strategy, three base-modulation pulses are needed for each cell operation in a CMLI. A sequential switching pulse (SSP) (A) is a square-wave signal with 50% duty ratio and half the fundamental frequency. This signal makes every power switch operating at MSPWM, and FPWM sequentially to equalize the power losses among the devices. FPWM (B) is a square-wave signal synchronized with the modulation waveform; $B = 1$ during the positive half cycle of the modulation signal, and $B = 0$ during negative half cycle. An SSP and FPWM pulses are same for all inverter cells. MSPWMs (C or D) for each cell, differs depends upon the type of carrier and modulation signals used. The block diagram representation of base modulator design is shown Fig. 4 (a)–(d). APOD modulation pulses for cell-I (C) is obtained from the comparison between unipolar modulation waveform and carrier, while APOD for cell-II (D) is generated from the comparison between modulation waveform and carrier with dc bias of $-V_c + 2A_c$. The modulation signals with dc bias of $-A_c$ are compared with single carrier to define SCSPWM pulses. CBSVM is based on a comparison of the modified sinusoidal reference ($V_a + V_{off} + V_{_off}$) with each carrier to determine the voltage level that the inverter should switch to. PSC pulses are based on the comparison of modulation waveform with the corresponding PSC waveform for every cell in a CMLI.

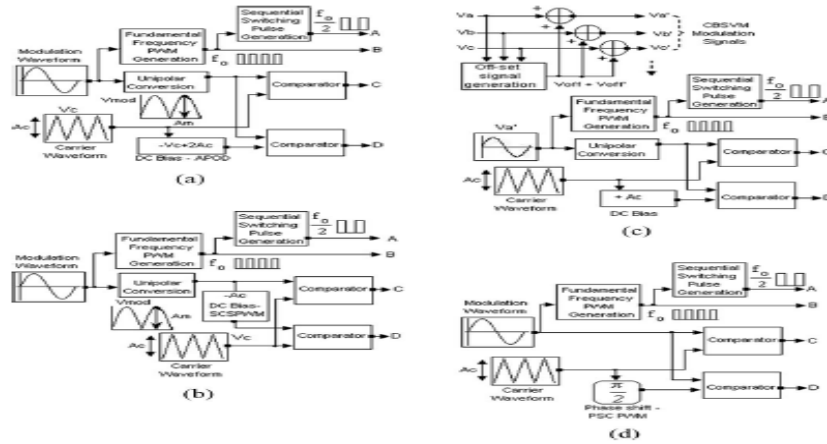


Fig. 4: Block diagram of five-level base modulator for: (a) HAPOD, (b) HSCSPWM, (c) HCBSVM, and (d) HPSC.

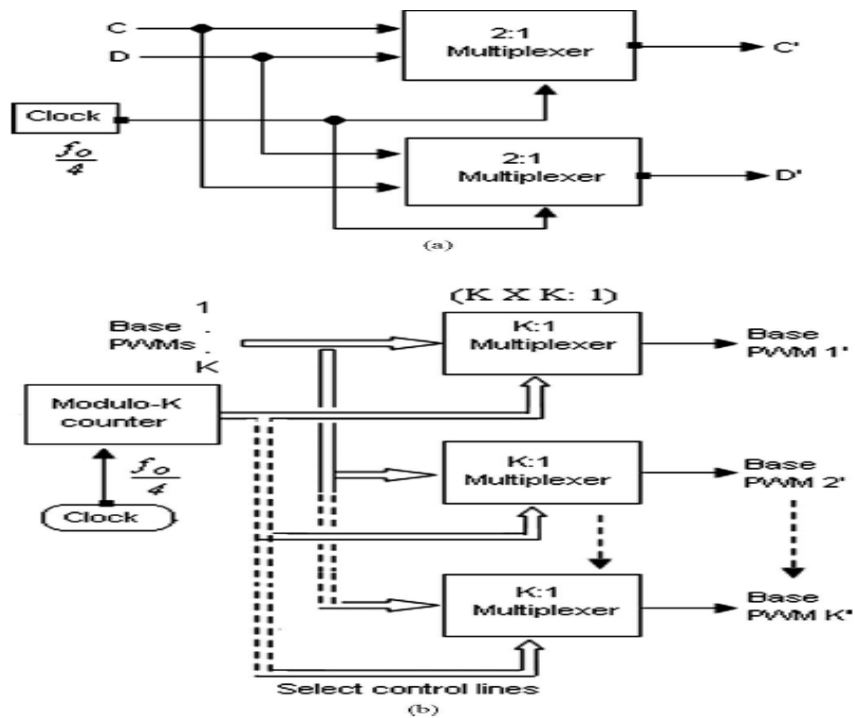


Fig. 5: Scheme of base PWM circulation: (a) five-level and (b) N-level operation.

(C) Base PWM Circulation

For long operating-time expectancy, it is important to share the power loss among every module, and furthermore, to every power device in the cell. This is one of the key issues the modulation should cover. A simple base PWM circulation scheme introduced here to get resultant HPWM circulation among the power modules. The scheme of five-level base PWM circulation is shown in Fig. 5 (a), consists of two 2:1 multiplexer, and selects one among the two PWMs based on the select clock signal. The clock frequency is $f_0/4$, makes the time base for PWM circulation from one module to another. After two fundamental frequency periods, the order is changed so that the first module HPWM becomes the second module, the second becomes the third, etc., while the last module HPWM shifts to the first. N-level PWM circulation scheme is presented in Fig. 5 (b), which consists of clock generator, modulo-K counter, and a multiplexer circuit. Modulo-K counter makes control signals for multiplexer to select appropriate input PWM channel. Multiplexer circuit consists of $(K \times K: 1)$ module for PWM selection, and it selects the PWM channel based on control signals. This PWM circulation

is based on simple multiplexer logic circuits, which makes the applicability of the algorithm very effective in a CPLD. The principle of the HPWM circulation is illustrated in Fig. 6, where the modules alternately participate in the HPWM operation and the corresponding phase voltage is presented at the same instant.

(D) Hybrid-Modulation Controller

HMC combines SSP, FPWM, and MSPWM that produces SSHM pulses. It is designed by using a simple combinational logic and the functions for a five-level HPWM are expressed as

$$\begin{aligned}
 S1 &= ABC' + \bar{A}B & S1' &= ABD' + \bar{A}B \\
 S2 &= \bar{A}BC' + \bar{A}\bar{B} & S2' &= \bar{A}BD' + \bar{A}\bar{B} \\
 S3 &= \bar{A}\bar{B}C' + \bar{A}\bar{B} & S3' &= \bar{A}\bar{B}D' + \bar{A}\bar{B} \\
 S4 &= \bar{A}BC' + AB & S4' &= \bar{A}BD' + AB
 \end{aligned}
 \quad \text{and}$$

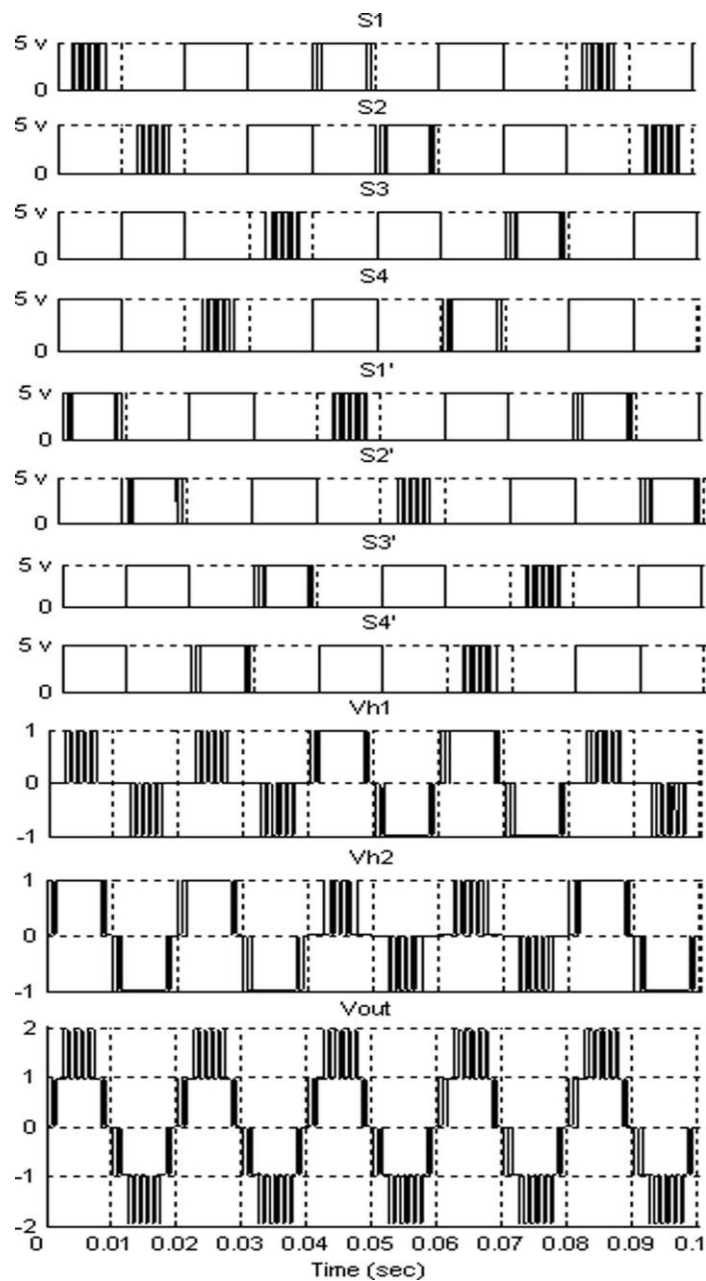


Fig 6: Five-level sequential switching HAPOD pulses.

Where A is an SSP, B is an FPWM, C₋ is an MSPWM for cell-I and D₋ is an MSPWM for cell-II. In Fig. 6, it is shown that each gate pulse is composed of both FPWM and MSPWM. If SSP A = 1, then S1, S2, S1₋, and S2₋ are operated with MSPWM, while S3, S4, S3₋, and S4₋ are operated at FPWM. If SSP A = 0, then S1, S2, S1₋, and S2₋ are operated at FPWM, while S3, S4, S3₋, and S4₋ are operated with MSPWM. Since A is a sequential signal, the average switching frequency amongst the four switches is equalized. Voltage stress and current stress of power switches in each cell is inherently equalized with this modulation. After every two fundamental periods, the HPWM pattern is changed so that the first module (S1, S2, S3, and S4) becomes the second module (S1', S2', S3', and S4'), and the second one shifts to the first, and is shown in Fig. 6. It can be observed from the waveforms of V_{h1} and V_{h2} that the implementation of HPWM circulation makes the inverter modules operate at same average switching frequency with the same conduction period. As a result, all inverter cells operate in a balanced condition with the same power-handling capability and switching losses. As it is concluded from Fig. 6, the resultant inverter switching is same as the type of MSPWM used.

IV. POWER LOSS ANALYSIS

The semiconductor power losses can be estimated from the characteristic curves, which are presented in the datasheets of each power device [18]. Only conduction and switching losses are considered here for power-loss estimation. The insulated gate bipolar transistors (IGBTs) selected are IRG4BC20SD, in which their maximum ratings are a forward current of 19A and a direct voltage of 600 V. The carrier frequency f_c is 1.5 kHz and each cell is connected to 100 V dc supply. The characteristics curves are $(V_{sat}(\theta) \times I_l(\theta))$ and $(E(\theta) \times I_l(\theta))$, where V_{sat} is the ON-state saturation voltage ($V_{ce}(\theta)$ for the IGBT and $V_F(\theta)$ for the diode); $E(\theta)$ represent the energy losses in one commutation (EON(θ) is a turn-ON commutation, EOFF(θ) is a turn-OFF commutation, and Erec(θ) is for diode reverse recovery process). Those curves are approximated by an exponential equation using curve-fitting tool of MATLAB

Mathematical models obtained for the IGBTs are given by

$$V_{ce} = 0.96e^{0.0016I_l(\theta)} - 0.4654e^{-0.044I_l(\theta)} \quad (12)$$

$$V_F = 0.6e^{0.002I_l(\theta)} - 0.4258e^{-0.0275I_l(\theta)} \quad (13)$$

$$E_{rec} = 0.00806e^{-0.000322I_l(\theta)} - 0.0057e^{-0.00446I_l(\theta)} \quad (14)$$

$$E_{ON} = 0.0041e^{0.0044I_l(\theta)} - 0.0037e^{-0.008I_l(\theta)} \quad (15)$$

$$E_{OFF} = 0.0443e^{0.00021I_l(\theta)} - 0.0547e^{-0.00107I_l(\theta)} \quad (16)$$

$$I_l(\theta) = I_{lmax} \sin(\theta - \phi) \quad (17)$$

ϕ is the load-displacement angle.

Switching losses are generated during the turn-ON and turn-OFF switching processes. The switching loss for every power device (P_{sw}) is obtained by identifying every turn-ON and turn OFF instants during one reference period as follows:

$$P_{sw} = 1/T (E_{ON} + E_{OFF} + E_{rec}).$$

Conduction losses are those that occur while the semiconductor device conducts current. It is computed by multiplying the ON-state voltage by ON-state current. The calculation of conduction losses for each semiconductor device is given by

$$P_{condT} = \int V_{ce}(\theta) I_l(\theta) V_{cm d}(\theta) d\theta$$

where $V_{cm d}(\theta)$ is the HPWM signal of the IGBT.

The power loss is the sum of switching and conduction losses. Fig. 7 (a) shows, for the full range of modulation index and the relative angle of the load currents, the switching-loss ratio of hybrid alternative phase opposition disposition (HAPOD) versus the conventional APOD techniques. It is noted that the surface is always below one, which means that the switching losses are significantly reduced. Fig. 7 (b) shows that the

conduction losses are higher. This is because of increased conduction period due to mixing of a FPWM, which is clearly shown in . Lastly, 7(c) shows the power-loss ratio between these two methods. Since the switching losses are predominant, the power losses of the proposed modulations are less than those conventional one. The mean value of the power-loss ratio surface is found 0.718 approximately, which means the power-loss reduction is about 28.2%. The best case is produced for a unity power factor and modulation index as one in which the loss saving is about 31%. Even though the power-loss ratio between HAPOD and its own APOD operations are presented, the other proposed modulations make similar power-loss saving with respect its own modulation techniques. In a practical high-power system, switching losses are higher than conduction losses. Therefore, saving switching losses becomes important to improve the efficiency of the system.

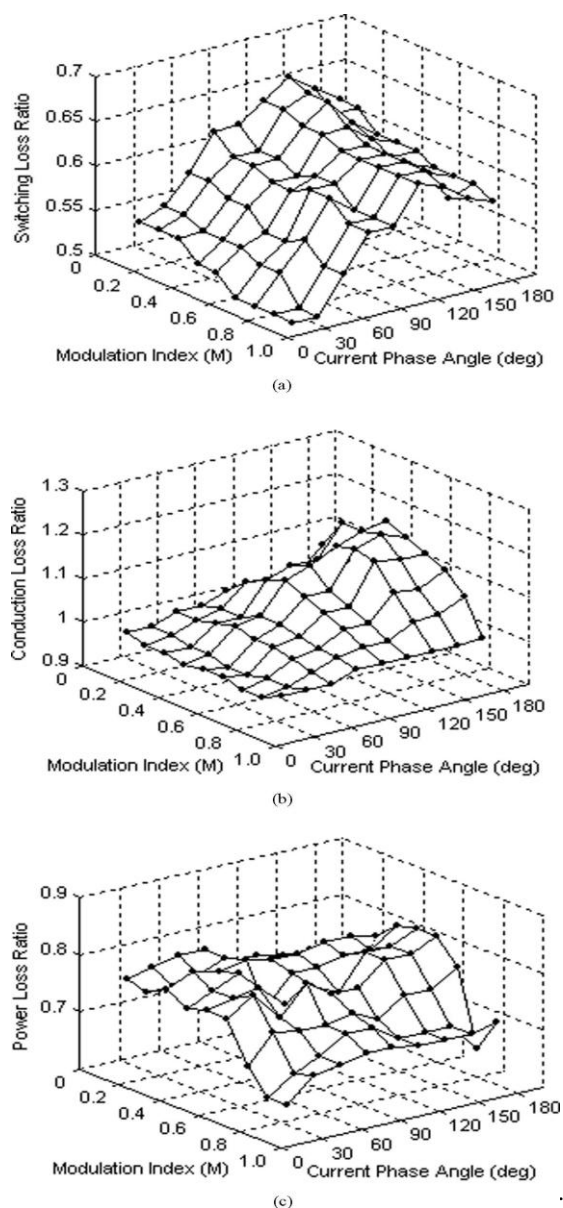


Fig 7: Loss-ratio analysis of HAPOD and APOD fed five-level Inverter
(a) Switching loss (b) conduction loss (c) power loss

(b)

V. SPECTRUM ANALYSIS OF OUTPUT VOLTAGE WAVEFORM

To evaluate the quality of the output voltage waveforms, the values of total harmonic distortion (THD) and weighted THD (WTHD) are calculated up to 50th order of harmonics, as suggested

in the IEEE standard 519

$$THD = \frac{\sqrt{\sum_{n=2}^{50} V_n^2}}{V_1} \quad (21)$$

$$WTHD = \frac{\sqrt{\sum_{n=2}^{50} \left(\frac{V_n}{n}\right)^2}}{V_1} \quad (22)$$

Where V_1 is the rms value of the fundamental component voltage, n is the order of harmonics, and V_n is rms value of the n th harmonic. It is found that the proposed modulations offer lower THD compared to the conventional one, thus the superiority. Furthermore, it is noted that higher the value of modulation index (M), lower the value of THD. Also, WTHD values are lower when the modulation index is closer to unity and when the carrier frequency increases. Throughout its linear modulation range, hybrid phase shifted carrier (HPSC) has the least harmonic distortion among SSHM schemes. In order to show the feasibility of the proposed modulations, the spectral analysis was performed by using MATLAB/Simulink software and is plotted in Fig. The load resistance and inductance are 10Ω and 15 mH , respectively, and the dc-bus voltage is set at 100 V . The frequency of modulated wave and carrier wave are 50 and 1500 Hz , respectively, and the inverter is operated with linear modulation region ($M = 0.85$). In Fig. (a) and (b), the harmonic cancellation up to the sidebands around the carrier frequency is achieved in the voltage waveform and the first significant harmonic is the 19th as predicted for HAPOD operation. In Fig.8.(c) and (d), the lower order harmonics are absent and the fundamental is controlled at the predefined value. It is interesting to note that the next significant harmonic will be 21st for HSCSPWM. The significant harmonics are 23, 29, 31, and 37, which are high frequency, with the rms values under 11% of the fundamental term. This inverter operates with odd frequency ratio, produces even sideband harmonics and for even frequency ratio, produces odd sideband harmonics. Furthermore, harmonics at the carrier and the multiples of carrier frequency do not exist at all. From the voltage spectrum in Fig.8 (e) and (f), the amplitude of the lower order harmonics are very low and same fundamental value is achieved. In Fig8 (g) and (h), complete harmonic cancellation of the switching harmonics up to $4fc$ carrier group sideband harmonics in the voltage is obtained, together with the expected cancellation of the triplen harmonics from the $4fc$ carrier group sidebands.

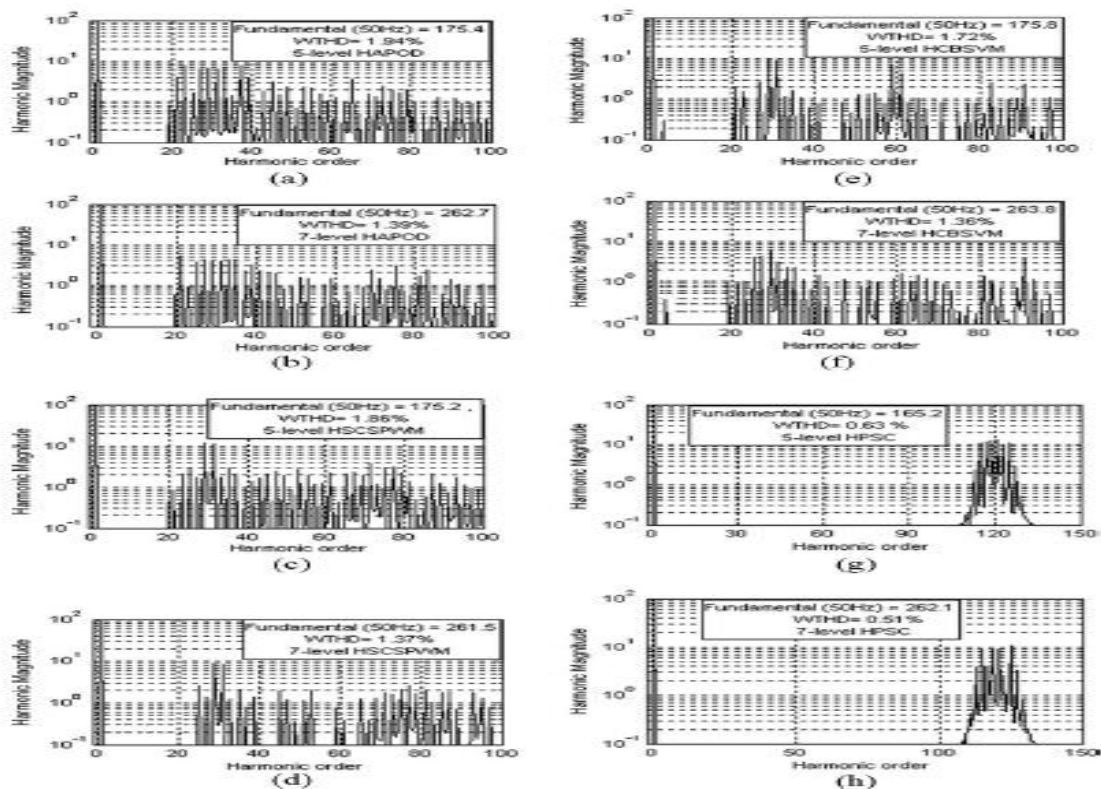


Fig 8. Harmonic spectra of the output voltage waveform in a linear modulation region

VI. CONCLUSION

In this paper, a new family of SSHM techniques for CMLI, operating at a lower switching frequency is proposed. The proposed technique is applied to well-known MSPWM schemes; APOD, PSC, CBSVM, and SCSPWM. Compared to conventional MSPWM schemes, less number of commutations and considerable switching-loss reduction is obtained while achieving the same fundamental voltage tracking. The harmonic performance of the SSHM schemes are analyzed in the entire range of modulation index and it seems to be good. An efficient sequential switching and PWM circulation techniques are embedded with these hybrid modulations for balanced power dissipation among the power devices within a cell and for series-connected cells. Combinational logic-based HMC is compact and easily realized with CPLD. These modulations can be easily extended to higher voltage level through the generalization process and implementation possible with existing CMLI structures. Analyses, simulations, and experimental results demonstrated the superiority of the proposed system.

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